REMARKS

Claims 1-33 are currently pending in the subject application and are presently under consideration. Claims 1-33 stand rejected. A clean version of all pending claims is found at pages 2-7.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

I. Rejection of Claims 1-33 Under 35 U.S.C. § 103(a)

Claims 1-33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Potter, *et al.* (US patent no. 6,157,393) (hereinafter "Potter") in view of Aranda (US patent no. 5,321,809). It is respectfully submitted that this rejection should be withdrawn for at least the following reasons. Neither Potter *et al.* nor Aranda, alone or in combination teach or suggest the claimed invention. Rather, the reference(s) teach away from the subject invention as recited in the rejected claims.

The Examiner has the burden under 35 U.S.C. §103 to establish a *prima facie* case of obviousness. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). To do that, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to successfully combine the relevant teaching of the references so that all claim limitations are suggested. *Id.*

M.P.E.P. 706.02(j) states:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."

With regard to claims 1, 21, 26 and 30 (and claims 2-20, 22-25, 27-29, and 31-33 which depend therefrom, respectively), the Examiner, citing Potter in view of Aranda,

states that "it would have been obvious to combine the teaching of Aranda to the system of Potter ..." However, neither Potter nor Aranda provide the necessary motivation to combine these references and, in fact, teach *away* from the present invention. Additionally, these references do *not* provide all the claim limitations of the present invention.

Potter discloses methods and apparatus for "directing graphical data toward a display device from a plurality of graphics processors ... in a manner that reduces the size of the interface on each graphics processor." (abstract, lines1-4) while the present invention discloses "*an improved raster engine with a multiple color depth digital display interface.*" (page 1, lines 6-7). Potter utilizes a clock cycle scheme to reduce the number of input pins on the output processor such that "during each clock cycle, the destination processor receives no more graphical data from the other processors than an amount equal to the product of the remaining number and the second amount." (col. 2, lines 2-6). The present invention employs a programmable control register, a dual port RAM and a logic device "*to remap the selected pixel data according to the selected display mode, and to provide remapped selected pixel data at the parallel output according to a universal routing scheme ....*"

The Examiner states that Potter teaches "*a raster engine for interfacing a frame buffer in a computer system to one of a plurality of disparate displays*" at (col. 3, lines 3-51). Applicants respectfully traverse this statement and request the Examiner to particularly point out where in (col. 3, lines 3-51) Potter discloses "*interfacing ... to one of a plurality of disparate displays.*" The Examiner also states that "*at least one control register programmable via the computer system to select a display mode*" is disclosed in Potter as element 125. Element 125 is "a bus controller 125 ... *provided for controlling a bus* 130." (col. 5, lines 66-67) (emphasis added). Thus, Potter teaches an element for controlling a bus 130, *not* a *control register for selecting a display mode* as found in the present invention. *Nor* does Potter teach a *programmable* control register for selecting a display mode as found in the present invention. Thus, Potter does *not* teach these aspects of the present invention.

The Examiner goes on to state that "*a logic device having a parallel output*" is disclosed at (col. 7, lines 50-67) in Potter. Applicants respectfully traverse this statement and request the Examiner to particularly point out where in (col. 7, lines 50-67) Potter discloses "*a logic device having a parallel output*." Potter teaches "a plurality of parallel gradient producing units 210" (col. 7, lines 53-54) and "parallel rasterizers 214" (col. 7, line 61) but does *not* teach "*a logic device having a parallel output*." Thus, Potter does *not* teach this aspect of the present invention.

The Examiner further states that "*the logic device being adapted to select appropriate pixel data from the dual port RAM device according to the selected display mode*" is found at (col. 8 line to col. 10, line 23; col. 14, lines 28-64; fig. 3a). These references to Potter disclose RAMDACS which convert digitally encoded images into analog signals that can be displayed by a monitor. The present invention states, "*the logic device being adapted to select appropriate pixel data from the dual port RAM device according to the selected display mode.*" Potter is outputting to the RAMDACs to convert digital signals to analog for a display. The present invention's logic device *receives* data *from* a dual port RAM device according to a selected display mode. Thus, Potter does *not* disclose this aspect of the present invention and actually *teaches away from* the present invention.

Examiner further continues stating that "*to remap the selected pixel data according to the selected display mode, and to provide remapped selected pixel data at the parallel output according to a universal routing scheme applicable to the plurality of disparate displays*" is found in Potter at (col. 10, line 7 to col. 13, line 65). Applicants respectfully traverse this statement and request the Examiner to particularly point out where in (col. 10, line 7 to col. 13, line 65) Potter discloses this. Potter teaches that "... graphical data is forwarded ... in a round robin manner" and that "this manner enables each RAMDAC ... to receive and/or forward the pixel data with a minimum number of pins." Potter is directed towards reducing pin count for display interfaces. The present invention is directed towards "*an improved raster engine with a multiple color depth digital display interface*." (page 1, lines 6-7) (emphasis added). The present invention states, "*The raster engine remaps the pixel data from the frame buffer format to an output*

format required by a selected display type according to a universal routing scheme, without requiring any rerouting of signals outside the raster engine." (page 11, lines 20-23) (emphasis added). The present invention also states, "*... the raster engine employs a universal routing scheme (e.g., as illustrated in the table 236)*" (page 40, line 8) (emphasis added). Additionally, the present invention states, "*While prior raster engines required rerouting of output signals outside of the raster engine, no such rerouting is required in order to employ the raster engine 2.*" (page 10, lines 10-12). Thus, Potter does *not* disclose these aspects of the present invention and actually *teaches away from* the present invention.

The Examiner does admit that, "... Potter fails to explicitly teach a dual port RAM device." The Examiner follows this with "On the other hand, Aranda specifically teaches a dual port RAM device for interfacing a frame buffer in a computer system." Applicants respectfully traverse this statement and request the Examiner to particularly point out where in Aranda "*a dual port RAM device operative to obtain pixel data from the frame buffer*" is disclosed. In the present invention, it states, "*a dual port RAM device operative to obtain pixel data from the frame buffer; and a logic device having a parallel output, the logic device being adapted to select appropriate pixel data from the dual port RAM device according to the selected display mode ....*" The Examiner continues with "it would have been obvious to combine the teaching of Aranda to the system of Potter because doing so would have enabled dividing the entire frame buffer into two separate devices so that the characteristics of adjacent pixels can be alternately stored in different ones of the two devices as noted in Aranda (col. 1, line 15 to col. 2, line 33)." Applicants respectfully point out that Aranda actually states, "The most straightforward approach to improving performance is to *divide the entire frame buffer into two separate devices* so that the characteristics of adjacent pixels can be alternately stored in different ones of the two devices." (col. 2, lines 22-26) (emphasis added). But, more importantly, Aranda then states, "The *difficulty with this approach*, however, is that twice the number of pins are required of the raster engine to access the dual devices. This requirement proves in practice to be a *significant complication*." (col. 2, lines 28-32) (emphasis added). Thus, Aranda actually *teaches away from* utilizing this approach.

Additionally, Aranda is disclosing using *two separate devices*, *not* a dual port RAM as found in the present invention.

The Examiner has *not* stated nor particularly pointed out any motivation or suggestion found in neither Potter nor Aranda to combine the references. *Nor* is there a reasonable expectation of success in combining the references as stated *supra*. Additionally, the references, separately or combined, neither teaches nor suggests all claim limitations of the present invention. For the above reasons, Examiner has *not* established a *prima facie* case of obviousness, and applicants respectfully request that the rejection be withdrawn.

II. Conclusion

The present application is believed to be in condition for allowance in view of the above amendments and comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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